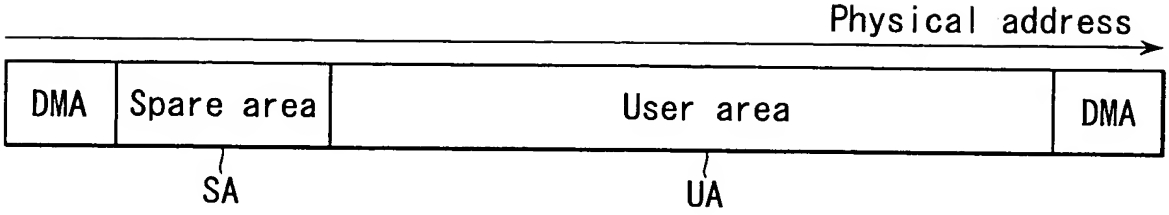


FIG. 1

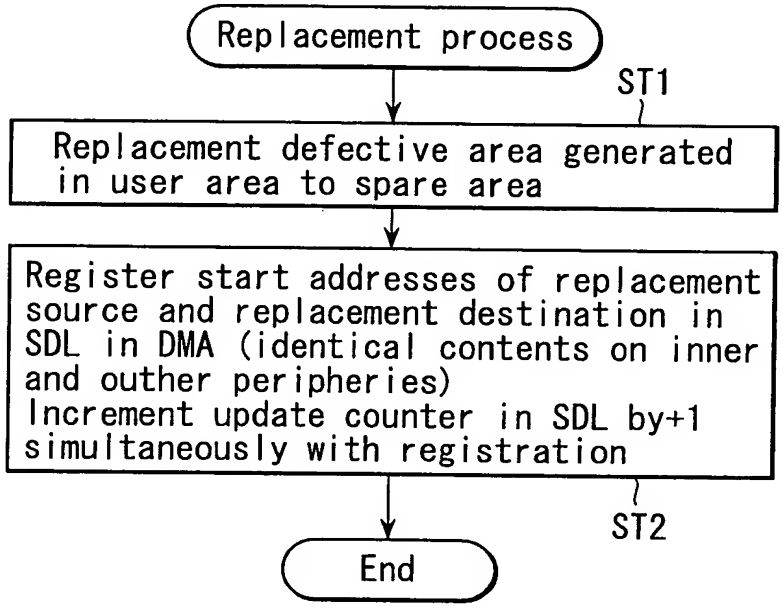


FIG. 2

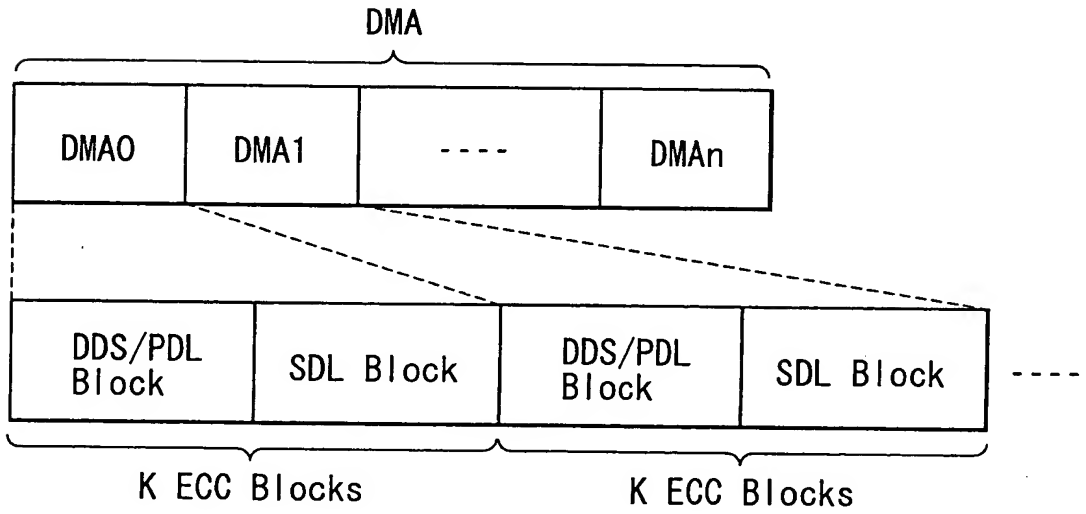


FIG. 3

DDS/PDL

BP	Contents	Number of bytes
0 to 1	DDS identifier (0A0Ah)	2 bytes
2	Reserved	1 byte
3	Disc certification flag	1 byte
4 to 7	DDS/PDL update counter	4 bytes
8 to 9	Number of Groups	2 bytes
10 to 11	Number of zones	2 bytes
12 to 79	Reserved	68 bytes
80 to 87	Location of Primary spare area	8 bytes
88 to 91	Location of LSN 0	4 bytes
92 to 255	Reserved	164 bytes
256 to 259	Start LSN for Zone 0	140 bytes
260 to 263	Start LSN for Zone 1	
----	----	
392 to 395	Start LSN for Zone 34	
396 to 399	DMA rec-counter 1	4 bytes
400 to 2047	reserved	1652 bytes

FIG. 4

SDL

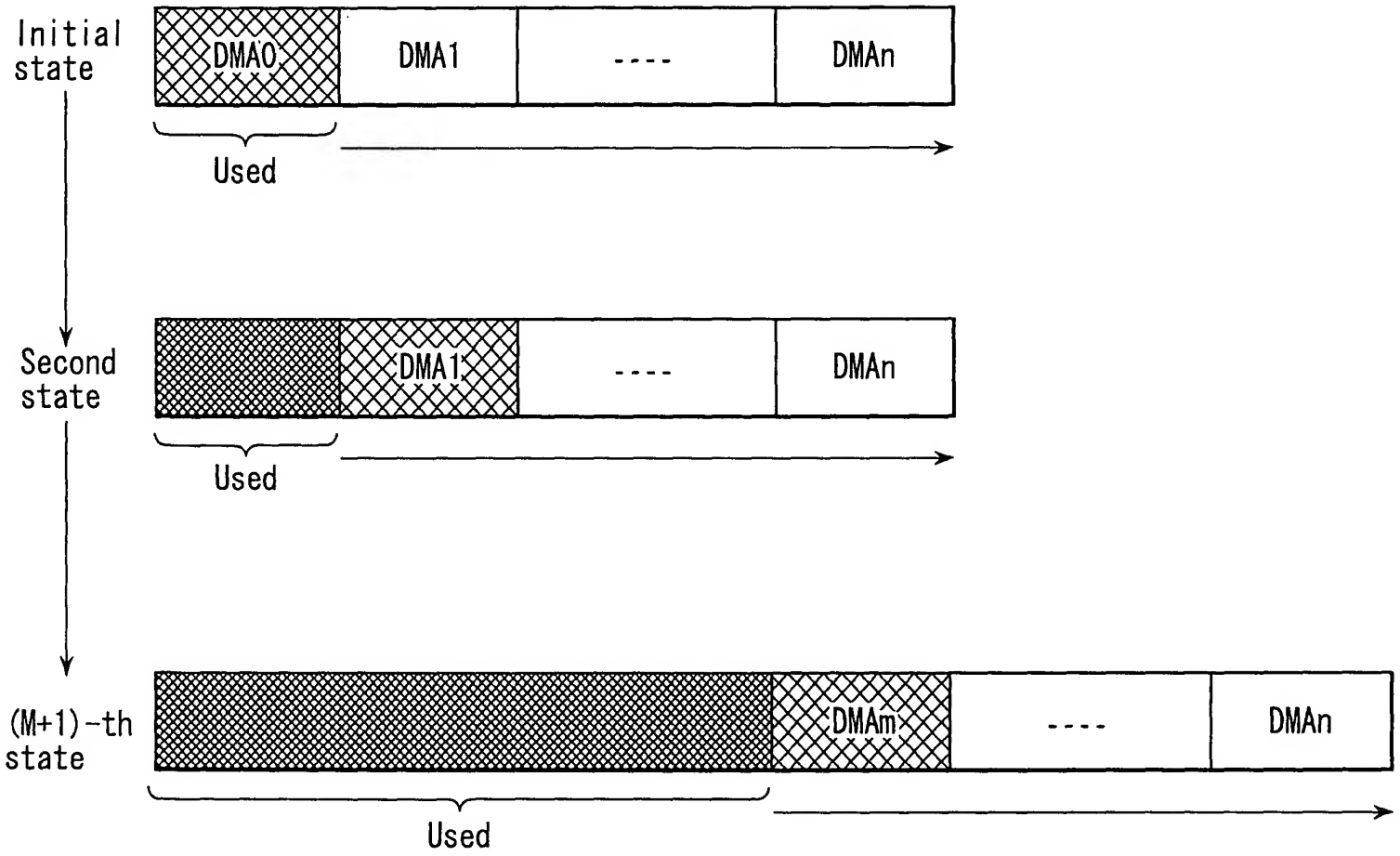
BP	Contents	Number of bytes
0 to 1	SDL identifier (0002h)	2 bytes
2 to 3	Reserved	2 bytes
4 to 7	SDL update counter	4 bytes
8 to 11	Start sector number of Supplementary spare area	4 bytes
12 to 15	Total number of logical sectors	4 bytes
16 to 19	DDS/PDL update counter	4 bytes
20	Spare area full flags	1 byte
21 to 24	DMA rec-counter 2	4 bytes
25 to 26	Number of entries in SDL	2 bytes
27 to 34	The first SDL entry	8 bytes
----	----	----
M to m+7	The last SDL entry	8 bytes

FIG. 5

SDL Entry

RSV (1B)	Replacement source address (3B)	RSV (1B)	Replacement destination address (3B)

FIG. 6


Initial state
DMA0
DMA1

DMAn
Used
Second state
DMA1

DMAn
Used
(M+1)-th state
DMAm

DMAn
Used

FIG. 7

DMA use state 1

	DDS/PDL update counter	SDL update counter	DMA counter
DMA 0	Normal use	Normal use	0～Nov-1
DMA 1	Continuing use of above value	Continuing use of above value	0～Nov-1
⋮	Continuing use of above value	Continuing use of above value	0～Nov-1
DMA m	Continuing use of above value	Continuing use of above value	0～Nov-1
⋮	Continuing use of above value	Continuing use of above value	0～Nov-1
DMA n	Continuing use of above value	Continuing use of above value	0～Nov-1

Nov:Allowable overwrite count

FIG. 8

DMA use state 2

	DDS/PDL update counter	SDL update counter	DMA counter
DMA 0	Normal use	Normal use	0～Nov-1
DMA 1	Normal use after reset	Normal use after reset	0～Nov-1
⋮	Normal use after reset	Normal use after reset	0～Nov-1
DMA m	Normal use after reset	Normal use after reset	0～Nov-1
⋮	Normal use after reset	Normal use after reset	0～Nov-1
DMA n	Normal use after reset	Normal use after reset	0～Nov-1

Nov:Allowable overwrite count

FIG. 9

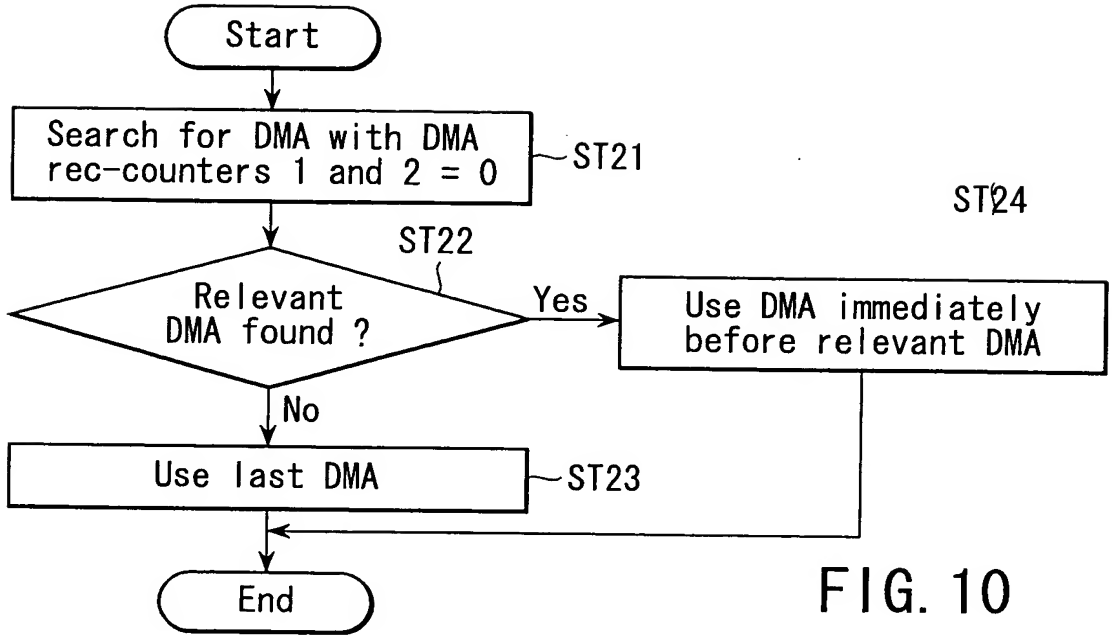

Start
Search for DMA with DMA rec-counters 1 and 2 = 0
ST21
ST22
Relevant DMA found ?
Yes
Use DMA immediately before relevant DMA
ST24
No
Use last DMA
ST23
End

FIG. 10

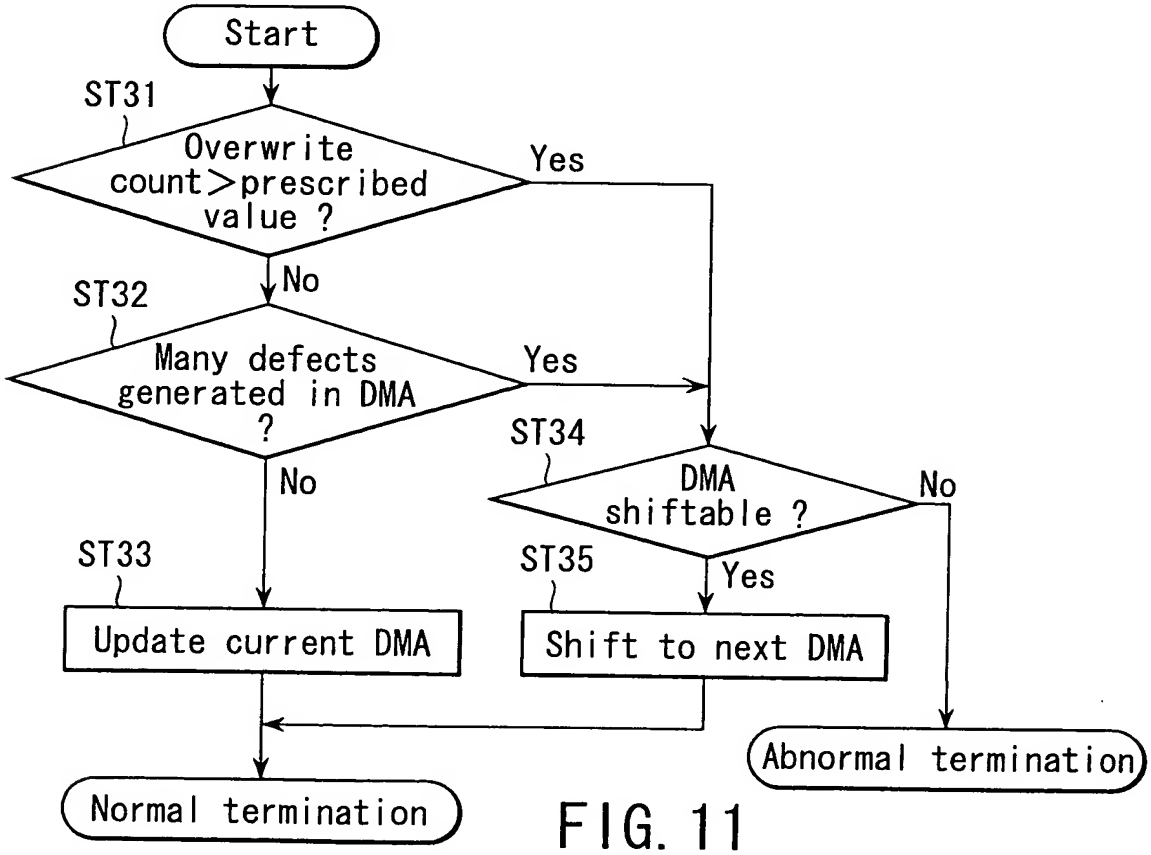
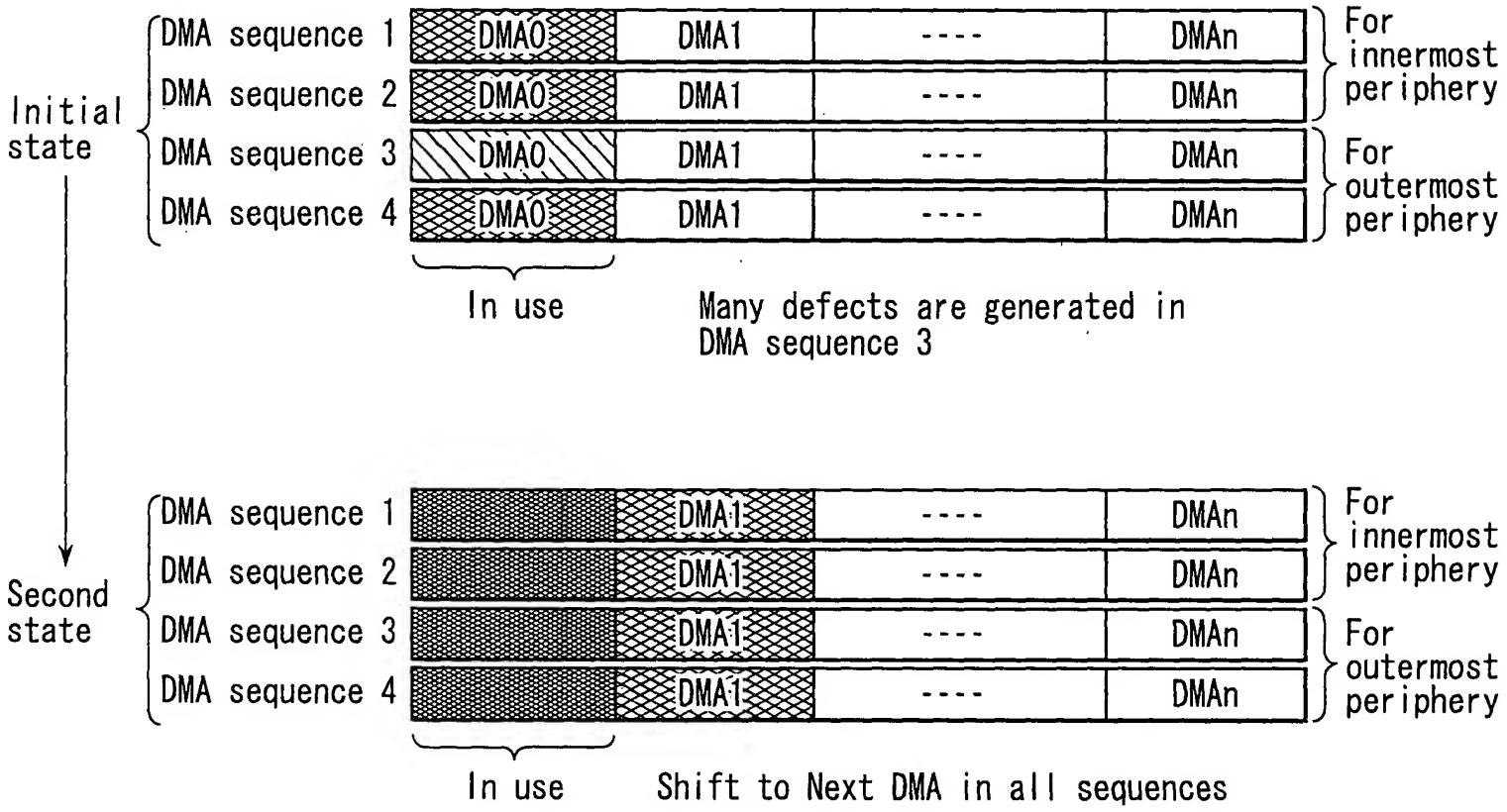

Start
ST31
Overwrite count>prescribed value ?
Yes
No
ST32
Many defects generated in DMA ?
Yes
No
ST34
DMA shiftable ?
No
Yes
ST33
ST35
Update current DMA
Shift to next DMA
Abnormal termination
Normal termination

FIG. 11


Initial state
DMA sequence 1
DMA sequence 2
DMA sequence 3
DMA sequence 4
DMA0
DMA1

DMAn
For innermost periphery
For outermost periphery
In use
Many defects are generated in DMA sequence 3
Second state
Shift to Next DMA in all sequences

FIG. 12

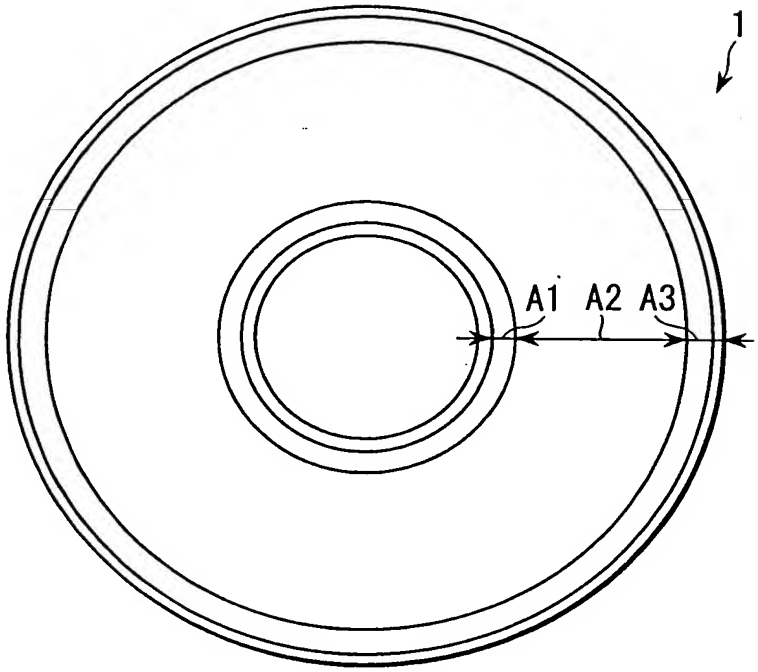

1
A1
A2
A3

FIG. 13

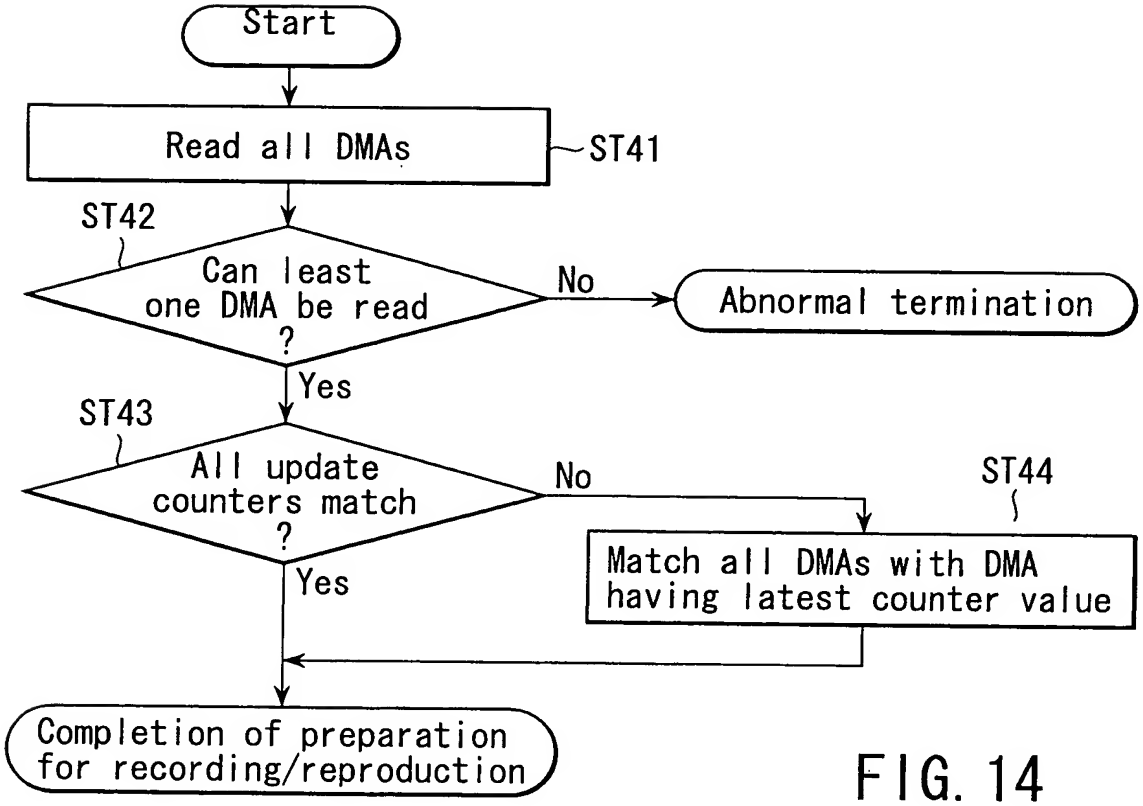

Start
Read all DMAs
ST41
ST42
Can least one DMA be read ?
No
Abnormal termination
Yes
ST43
All update counters match ?
No
ST44
Match all DMAs with DMA having latest counter value
Yes
Completion of preparation for recording/reproduction

FIG. 14

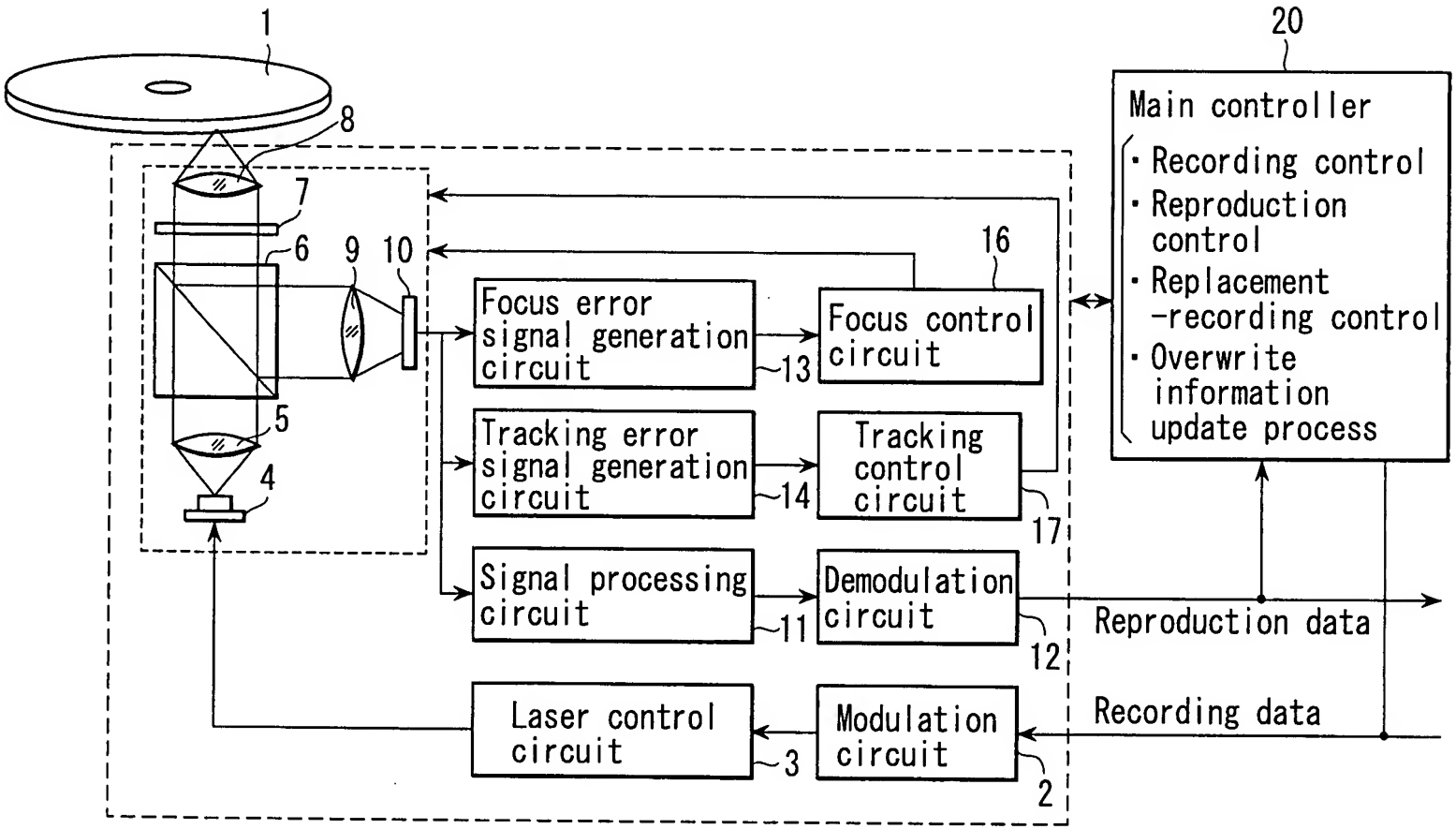

1
20
Main controller
• Recording control
• Reproduction control
• Replacement -recording control
• Overwrite information update process
8
7
6
9
10
16
Focus error signal generation circuit
13
Focus control circuit
5
Tracking error signal generation circuit
14
Tracking control circuit
17
4
Signal processing circuit
11
Demodulation circuit
12
Reproduction data
Laser control circuit
3
Modulation circuit
2
Recording data

FIG. 15